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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,561	03/18/2004	S. Brandon Keller	200311778-1	5956

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EXAMINER	
TO, TUYEN P	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,561	KELLER ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	77

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 03/18/2004. Claims 1-30 are pending.

Claim Objections

1. **Claims 11, 20, and 29** are objected to because of the following informalities: the recited " most likely" in the claims is not a definite claim language. Appropriate correction is required.

2. **Claims 13 and 22** are objected to because of the following informalities: the recited " and " in claim 13 (line 6) and in claim 22 (line 9) appears to be a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-2, 7, 11-13, 16, 20-22, 25, and 29-30** are rejected under 35 U.S.C. 102(b) as being anticipated by Pileggi et al. (US Patent No. 6286128).

Referring to claim 1, Pileggi et al. disclose a method, a system (claim 13), and a computer-readable medium (claim 22) for controlling analysis by an analysis tool of multiple instantiations of a circuit in a hierarchical circuit design, the method comprising:

providing a user-selected analysis option to the analysis tool (Pileggi et al., col. 4, ll. 57- col. 5, ll. 49);

analyzing a first instantiation of the circuit as specified by the analysis option (Pileggi et al., col. 4, ll. 57-col. 5, ll. 49); and

responsive to the first instantiation of the circuit passing the analysis, terminating analysis of the circuit (Fig. 1B; col. 12, ll. 60 - col. 13, ll. 45).

5. **Referring to claim 13 and similarly recited claim 22**, Pileggi et al. disclose a system / computer-readable medium (claim 22) for analyzing multiple instantiations of a circuit in a hierarchical circuit design, the system comprising:

means for receiving a user-selected analysis option (Pileggi et al., col. 4, ll. 57-col. 5, ll. 49);

means for analyzing a first instantiation of the circuit as specified by the analysis option (Pileggi et al., col. 4, ll. 57-col. 5, ll. 49); and

means responsive to the first instantiation of the circuit passing the analysis for terminating analysis of the circuit (Fig. 1B; col. 12, ll. 60 - col. 13, ll. 45); and

means for providing results of the analysis (col. 13, ll. 6-23, see "timing constraint violations" (analysis result)).

Referring to claim 2, Pileggi discloses the method of claim 1 further comprising providing results of the analysis (col. 13, ll. 6-23, see "timing constraint violations" (analysis result)).

Referring to claim 7 and similarly recited claims 16 and 25, Pileggi et al. disclose the method of claim 1 wherein the first instantiation of the circuit comprises a

composite worst case instantiation of the circuit, the method further comprising determining a composite worst case instantiation of the circuit (Pileggi, col. 12, ll. 48-54).

Referring to claim 11 and similarly recited claims 20 and 29, Pileggi et al. disclose the method of claim 1 wherein the first instantiation of the circuit comprises the one of the instantiations of the circuit most likely to fail analysis (Pileggi et al., col. 4, ll. 57-col. 5, ll. 49).

Referring to claim 12 and similarly recited claims 21 and 30, Pileggi et al. disclose the method of claim 1 wherein the first instantiation of the circuit is a user-selected one of the instantiations (Pileggi et al., col. 4, ll. 57-col. 5, ll. 49).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 3-4, 14, and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi et al. in view of Singhal et al. (US Pub. No. 2003/0208730).

Referring to claim 3 and similarly recited claims 14 and 23, Pileggi et al. disclose substantially all the elements in the claims 3, 14, and 23 **except** responsive to the first instantiation of the circuit failing the analysis, terminating analysis of the circuit.

Singhal et al. disclose the step of responsive to the first instantiation of the circuit failing the analysis, terminating analysis of the circuit (Singhal et al. , Fig. 7-9, p.5[0066]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Pileggi et al. with the teachings disclosed by Singhal et al. because the combined method would permit complete control over a region of the circuit model to be examined while checking for a particular property and that does not involve any modification of the design (p.2 [0016])

Referring to claim 4, the method of claim 3 further comprising providing results of the analysis (Singhal et al., p.2 [0023]).

8. **Claims 5-6 and similarly recited claims 15 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi et al. in view of Burks et al. (US Pub. No. 2004/0078767).

Referring to claim 5 and similarly recited claims 15 and 24, Pileggi et al. disclose substantially all the elements in the claims 5, 15, and 24 **except** responsive to the first instantiation of the circuit failing the analysis, analyzing all remaining instantiations of the circuit.

Burks et al. disclose the step of responsive to the first instantiation of the circuit failing the analysis, analyzing all remaining instantiations of the circuit (Figs. 1-2, p. 1[0012], p.2[0035], and p. 3[0049]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Pileggi et al. with the teachings disclosed by Burks et al. because such modification would provide a method that can run analysis to verify each block hierarchically (Fig. 2, element 255; p. 2[0028]).

Referring to claim 6, the method of claim 5 further comprising providing results of the analysis (Burks et al., and p.3 [0049]).

9. **Claim 10 and similarly recited claims 19 and 28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi et al. in view of Naffziger et al. (US Pub. No. 2003/0115560)

Pileggi et al. disclose substantially all the elements in the claims 10, 19, and 28 **except** further comprising selecting a maximum drive fight scale factor and assigning the maximum drive fight scale factor to the composite worst case instantiation.

Naffziger et al. disclose the step of selecting a maximum drive fight scale factor (p. 1[0014], p.3[0063]-[0064]) and assigning the maximum drive fight scale factor to the composite worst case instantiation (p.3[0034]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Pileggi et al. with the teachings disclosed by **Naffziger et al.** because such modification would provide a method for performing limited modifications to one or more critical circuit in a control manner (p. 1[0005]).

10. **Claims 9, 18, and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi et al. in view of Cirit (US Pub. No. 2002/0188918).

Pileggi et al. disclose substantially all the elements in the claims 9, 18, and 27 except for each driver in the circuit, selecting an input and output slope combination for the driver that maximizes a crossover current for a signal driven by the driver and assigning the selected input and output slope combination to the driver in the composite worst case instantiation.

Cirit discloses for each driver in the circuit, selecting an input and output slope combination for the driver that maximizes a crossover current for a signal driven by the driver and assigning the selected input and output slope combination to the driver in the composite worst case instantiation (p. 2[0011]-[0014] and p. 4[0041]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Pileggi et al. with the teachings disclosed by **Cirit** because such modification would provide a timing optimization and placement method where it can be performed independently in the most efficient manner (p.1[0010]).

11. **Claim 8 and similarly recited claims 17 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Pileggi et al. in view of Raman et al. (US Pat. No. 5,535,370).

Pileggi et al. disclose substantially all the elements in the claims 8, 17, and 26 **except** wherein the determining the composite worst case instantiation of the circuit comprises for each net in the circuit:

selecting one of the instantiations having a highest activity factor for the net and assigning the highest activity factor to the net of the composite worst case instantiation;

selecting a logic configuration set that provides a maximum possible switching states for the circuit and assigning the logic configuration to the composite worst case instantiation; and

selecting a maximum of any scale factors that increase loading on signals in the circuit and assigning the selected scale factors to the composite worst case instantiation.

Raman et al. disclose wherein the determining the composite worst case instantiation of the circuit comprises for each net in the circuit:

selecting one of the instantiations having a highest activity factor for the net and assigning the highest activity factor to the net of the composite worst case instantiation (col. 1, ll. 42-col. 2, ll. 31; col. 3, ll. 6 – col. 4, ll. 5);

selecting a logic configuration set that provides a maximum possible switching states for the circuit and assigning the logic configuration to the composite worst case instantiation (col. 1, ll. 42-col. 2, ll. 31; col. 3, ll. 6 – col. 4, ll. 5); and

selecting a maximum of any scale factors that increase loading on signals in the circuit and assigning the selected scale factors to the composite worst case instantiation (col. 1, ll. 42-col. 2, ll. 31; col. 3, ll. 6 – col. 4, ll. 5).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Pileggi et al. with the teachings disclosed by Raman et al. because such modification would provide a method and system for calculating realistic current and power analysis (abstract; col. 1, ll. 42-49).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To

Patent Examiner

AU 2825

PAUL DINH
PRIMARY EXAMINER